IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Reissue Application of	
Amos Intrater et al.	**DECLARATION OF MOSHE DORON**
Patent No. 5,630,153	
Issued: May 13, 1997	2001 Ferry Building San Francisco, CA 94111 (415) 433-4150
For: **INTEGRATED DIGITAL SIGNAL PROCESSOR/GENERAL PURPOSE CPU WITH SHARED INTERNAL MEMORY**	Attorney Docket No: NSC8-8400

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

I, Moshe Doron, hereby declare that:

1. This declaration is directed to U.S. Patent No. 5,630,153 (the '153 patent), which issued on May 13, 1997.

2. My residence and post office address are both 7 Hashachar St., Raanana, 43564 Israel. I am a citizen of Israel.

3. I am a joint inventor of the invention recited in the claims of the '153 patent. The names, addresses, and citizenships of my co-inventors are:

a. Gideon Intrater. The residence and post office address of Gideon Intrater are both 1035 Aster Ave., Sunnyvale, CA 94086. Gideon Intrater is an Israeli citizen.

b. Amos Intrater. The residence and post office address of Amos Intrater are both 81 Emek Hefer St., Netanya, 42220 Israel. Amos Intrater is an Israeli citizen.

c. Lev Epstein. The residence and post office address of Lev Epstein are both 13A Admonit St., Ramat Poleg, Netanya, Israel. Lev Epstein is an Israeli citizen.

d. Maurice Valentaten. The residence and post office address of Maurice Valentaten are both Kurt Huber Ring 3, 82256 Fuerstenfeldbruck, Germany. Maurice Valentaten is a Belgian citizen.

e. Israel Greiss. The residence and post office address of Israel Greiss are both 48 Rambam St., Raanana, 43602 Israel. Israel Greiss is an Israeli citizen.

4. I hereby state that I have reviewed and understand the contents of the specification of the '153 patent, including the claims, as amended by any amendments specifically referred to in this declaration.

5. I believe my co-inventors and I are the original and first inventors of the subject matter which is described and claimed in the '153 patent for which a reissue patent is sought.

6. I acknowledge the duty to disclose to the Office all information known to me to be material to patentability as defined in Title 37 of the Code of Federal Regulations (CFR) §1.56.

7. I hereby state that one error that is being relied upon as the basis for reissue is that claims 1, 9, and 10 of the '153 patent appear to read on page 12 and Chapter 13, titled TMS32020 and MC68000 Interface, by Charles Crowell, of Digital Signal

Processing Applications with the TMS320 Family, Volume I, Edited by Kun-Shan Lin, Ph.D., dated September 1986, which has not been previously considered by the Patent Office. Page 12 and the Crowell chapter of the Digital Signal Processing Applications (DSPA) document came to our attention after issuance of the '153 patent. A copy of page 12 and the Crowell chapter from the DSPA document are attached in an accompanying IDS.

Page 12 and the Crowell chapter from the DSPA document cited in the IDS are from a June 1989 reprint. I understand that the assignee of the '153 patent, National Semiconductor, has searched for the 1986 document, but has been unable to find it. Although page 12 and the Crowell chapter of the DSPA document cited in the IDS are from a June 1989 reprint, I believe that page 12 and the Crowell chapter of the June 1989 DSPA document are an exact copy of page 12 and the Crowell chapter of the September 1986 DSPA document because the June 1989 reprint was not separately copyrighted, and was printed with 1986 dates throughout the document. I do not believe that documents with a June 1989 publication date are prior art with respect to the '153 patent because my co-inventors and I have an earlier date of conception.

Since claims 1, 9, and 10 appear to read on page 12 and the Crowell chapter of the DSPA document, I believe the original patent to be wholly or partly inoperative or invalid by reason of my co-inventors and I claiming more than we had a right to claim.

Specifically, claim 1 of the '153 patent requires:

> "a shared bus for transferring both data and instructions; [and]

> "a shared memory array for storing both data and general purpose instructions and that is connected for transfer of both data and general purpose instructions between the shared bus and the shared memory array". [Brackets added].

In the schematic diagrams shown on pages 376-377, the Crowell document discloses an address bus A BUS and a data bus D BUS for transferring both data and instructions. In addition, on page 372, column 1, line 11, the Crowell document teaches that the IMS1421-40 chips are shared memories which, as shown on page 377, are connected to the shared bus (the address and data buses A BUS and D BUS). Further, on page 371, in the System Configuration section, Crowell discloses that the shared memories (the IMS1421-40 ships) store both data and instructions.

Claim 1 of the '153 patent also requires:

> "a digital signal execution unit connected to the shared bus for processing the digital signal utilizing both data transferred between the shared memory array and the digital signal execution unit on the shared bus and a selected sequence of individual digital signal processor (DSP) instructions, the selected sequence of DSP instructions consisting of individual general purpose instructions transferred between the shared memory array and the digital signal execution unit on the shared bus".

On page 373, under the Summary section, Crowell teaches that the TMS32020 chip is a digital signal processor (DSP) which, as shown on page 377, is connected to the shared memories (the IMS1421-40 chips) via the shared bus (the address and data buses A BUS and D BUS). Further, on page 371, in the System Configuration section, Crowell discloses that both instructions and data are transferred to the

shared memories (the IMS1421-40 chips) for use by the DSP (the TMS32020 chip).

Claim 1 of the '153 patent further requires:

> "a general purpose processor connected to the shared bus for controlling the digital signal execution unit by selecting each general purpose instruction to be transferred to the digital signal execution unit from the shared memory array,
>
> "whereby the selected sequence of individual DSP instructions executed by the digital signal execution unit is selectively configurable by the general purpose processor."

On page 371, in the Introduction section, Crowell discloses that the MC68000 chip is a host processor, while on page 372, column 1, line 9, Crowell teaches that the 74LS241 chips are buffers.

On pages 376-377, Crowell's schematic diagrams show that the address and data lines from the MC68000 processor are connected to the shared bus (the address and data buses A BUS and D BUS) via the buffers (the 74LS241 chips). Thus, when the 74LS241 buffers are turned on, the MC68000 processor is connected to the shared bus (the address and data buses A BUS and D BUS).

In addition, on page 371, in the System Configuration section, Crowell discloses that both instructions and data are transferred from the 68000 host processor to the shared memories (the IMS1421-40 chips), and then to the DSP (the TMS32020 chip). Thus, claim 1 of the '153 patent appears to read on the Crowell document.

With respect to independent claim 9 of the '153 patent, this claim requires:

> "(a) a digital signal execution unit that recovers digital data from the digital signal by

executing a selected sequence of digital signal processor (DSP) instructions;

(b) a general purpose processor that selects the sequence of DSP instructions for execution by the digital signal execution unit from a set of DSP instructions and that performs general purpose processing tasks by executing general purpose instructions utilizing selected data;

(c) a shared internal bus for transferring both data and instructions and to which both the digital signal execution unit and the general purpose processor are connected; and

(d) a shared internal memory array connected to the shared internal bus via an internal input/output port of the shared internal memory array such that the shared internal memory array is accessible by the digital signal execution unit via the internal input/output port for transferring operands utilizable by the digital signal execution unit between the shared internal memory array and the digital signal execution unit on the shared internal bus and such that the shared internal memory array is accessible by the general purpose processor via the internal input/output port for transferring the general purpose instructions and the selected data between the shared internal memory array and the general purpose processor on the shared internal bus;"

The above discussion with respect to the digital signal execution unit, the general purpose processor, the shared internal bus, and the shared internal memory array of claim 1 also apply to claim 9.

Claim 9 of the '153 patent further requires:

"wherein the digital signal execution unit includes an internal address generator for retrieving operands from the shared internal memory array via the shared internal bus for use by the digital signal execution unit in executing the selected sequence of DSP instructions."

On page 12 of the DSPA document, which shows the internal core of the TMS32020 chip, the registers

which are labeled ARO(16), AR1(16), AR2(16), AR3(16), and AR4(16) function as an internal address generator as required by claim 9. Thus, claim 9 of the '153 patent appears to read on page 12 and the Crowell chapter of the DSPA document.

With respect to independent claim 10 of the '153 patent, elements (a), (b), (c), and (d) are the same as the corresponding elements in claim 9. Thus, the above discussion with respect to the digital signal execution unit, the general purpose processor, the shared internal bus, and the shared internal memory array of claim 1 also apply to claim 10.

Claim 10 of the '153 patent further requires:

> "(e) an instruction sequencing unit connected to the shared internal bus for controlling the flow of execution of the DSP instructions and the general purpose instructions."

Although the Crowell document does not explicitly show this unit, it is believed that one skilled in the art would understand that the MC68000 chip has circuitry which performs this function. Thus, claim 10 of the '153 patent further appears to read on the Crowell document.

As a result, claims 1, 9, and 10 are cancelled in this reissue application.

8. I hereby further state that a second error that is being relied upon as a basis for reissue is that none of the claims in the '153 patent provide coverage of the scope provided by new reissue claims 11-44. As a result, I believe the original patent to be wholly or partly inoperative or invalid by reason of my co-inventors and I claiming less than we had a right to claim.

New independent reissue claims 11, 20, and 29 define the invention as follows:

> 11. A data processing system comprising:
> a first bus;
> a memory connected to the first bus;
> a general purpose processor (GPP) connected to the first bus, the GPP loading operands into the memory; and
> a digital signal processor (DSP) connected to the first bus, the DSP having a register and starting execution of an instruction in response to the GPP loading information into the register.

> 20. A data processing system comprising:
> a first bus;
> a memory connected to the first bus;
> a general purpose processor (GPP) connected to the first bus, the GPP loading operands into the memory; and
> a digital signal processor (DSP) connected to the first bus, the DSP having a register and executing an instruction in response to the GPP loading information into the register, the information loaded into the register identifying the instruction.

> 29. A data processing system comprising:
> a first bus;
> a memory connected to the first bus;
> a general purpose processor (GPP) connected to the first bus, the GPP loading operands into the memory; and
> a digital signal processor (DSP) connected to the first bus, the DSP having a register, executing an instruction in response to the GPP loading information into the register, and retrieving operands required by the instruction from the memory by processing the information loaded into the register.

Support for new claims 11, 20, and 29 may be found in FIG. 3, in column 6, lines 37-67, column 8, lines 25-53, and column 9, lines 55-65 of the '153 patent specification.

None of the existing claims provide a scope of coverage which is the same as, or comparable to, the

scope of coverage now provided by new reissue claims 11, 20, and 29. Independent claim 4 and dependent claims 5-6 are the only existing claims that recite a DSP which has a register (a control register). Claims 4-6, however, do not recite that the GPP loads operands into the memory.

In addition, none of the previously submitted claims provided a scope of coverage which is the same as, or comparable to, the scope of coverage now provided by new reissue claims 11, 20, and 29. The only previously submitted claims which recite a DSP that has a register are independent claim 10 and dependent claims 11-14 in the originally-filed application (Application Serial No. 07/467,148 filed on January 18, 1990).

Independent claim 10, in addition to reciting a register, also recited an internal memory that provided storage for data retrieved by the GPP. Originally-filed claim 10, however, further recited a number of elements which are not present in new reissue claims 11, 20, and 29; namely a bus interface unit and an external memory. Thus, originally-filed claims 10-14 did not provide a scope of coverage which is the same as, or comparable to, new reissue claims 11, 20, and 29.

Subsequently, originally-filed claim 10 was amended in a Preliminary Amendment filed on January 29, 1993 as part of an FWC application (Application Serial No. 08/011,102 filed on January 29, 1993). The amendment added limitations to originally-filed claim 10, and deleted the bus interface unit, the external memory, and reference to the internal memory providing storage for data retrieved by the GPP.

In addition, dependent claim 11 was also amended to add further limitations to the multiplier/

accumulator unit, while claims 13 and 14 were cancelled (dependent claim 12 further defines the address generator of original claim 10). Thus, claims 10-11, as amended, and claim 12 did not provide a scope of coverage which is the same as, or comparable to, new reissue claims 11, 20, and 29.

Following this, amended claim 10 was cancelled in favor of claim 27 in the Amendment filed on January 7, 1994. In addition, claims 11-12 were amended to further recite the multiply/accumulate unit, and the address generator. Claims 27 and 11-12, in turn, subsequently issued as claims 4-6, respectively, of the '153 patent.

Therefore, none of the existing claims, and none of the previously presented claims, provide a scope of coverage which is the same as, or comparable to, the scope of coverage now provided by new reissue claims 11, 20, and 29.

New dependent reissue claims 12-19, 21-28, and 30-36 further recite the invention as follows:

> 12. The data processing system of claim 11 wherein the operands held in the memory are randomly accessible.
>
> 13. The data processing system of claim 11 wherein the information placed in the register identifies the instruction to be executed.
>
> 14. The data processing system of claim 11 wherein the DSP is connected to the memory via a second bus.
>
> 15. The data processing system of claim 11 wherein the DSP places the GPP in a continuous wait state while the DSP executes the instruction.
>
> 16. The data processing system of claim 11 wherein the GPP reads a status of the DSP after the DSP completes execution of the instruction.

17. The data processing system of claim 11 wherein the GPP reads a value that results from executing the instruction after the DSP completes execution of the instruction.

18. The data processing system of claim 11 wherein the DSP only executes a single instruction when said information is loaded into the register.

19. The data processing system of claim 11 wherein the DSP retrieves the operands from the memory.

21. The data processing system of claim 20 wherein the operands held in the memory are randomly accessible.

22. The data processing system of claim 20 wherein the information placed in the register identifies the instruction to be executed.

23. The data processing system of claim 20 wherein the DSP is connected to the memory via a second bus.

24. The data processing system of claim 20 wherein the DSP places the GPP in a continuous wait state while the DSP executes the instruction.

25. The data processing system of claim 20 wherein the GPP reads a status of the DSP after the DSP completes execution of the instruction.

26. The data processing system of claim 20 wherein the GPP reads a value that results from executing the instruction after the DSP completes execution of the instruction.

27. The data processing system of claim 20 wherein the DSP only executes a single instruction when said information is loaded into the register.

28. The data processing system of claim 20 wherein the DSP retrieves the operands from the memory.

30. The data processing system of claim 29 wherein the operands held in the memory are randomly accessible.

31. The data processing system of claim 29 wherein the information placed in the register identifies the instruction to be executed.

32. The data processing system of claim 29 wherein the DSP is connected to the memory via a second bus.

33. The data processing system of claim 29 wherein the DSP places the GPP in a continuous wait state while the DSP executes the instruction.

34. The data processing system of claim 29 wherein the GPP reads a status of the DSP after the DSP completes execution of the instruction.

35. The data processing system of claim 29 wherein the GPP reads a value that results from executing the instruction after the DSP completes execution of the instruction.

36. The data processing system of claim 29 wherein the DSP only executes a single instruction when said information is loaded into the register.

Support for new reissue claims 12, 21, and 30 may be found in column 6, lines 5-7 of the '153 patent specification. Support for new reissue claims 13, 22, and 31 may be found in column 6, lines 47-50 and column 9, lines 55-57 of the '153 patent specification. Support for new reissue claims 14, 23, and 32 may be found in FIG. 3 of the '153 patent specification. Support for new reissue claims 15, 24, and 33 may be found in column 6, lines 50-53 of the '153 patent specification. Support for new reissue claims 16-18, 25-27, and 34-36 may be found in column 6, lines 54-67 of the '153 patent specification. Support for new reissue claims 19 and 28 may be found in column 6, lines 45-46.

Since existing claims 4-6 fail to recite that the GPP loads operands into the memory, none of the existing claims provide a scope of coverage which is

the same as, or comparable to, the scope of coverage now provided by new reissue claims 12-19, 21-28, and 30-36.

In addition, since originally-filed claims 10-14 recited elements which are not recited in new reissue claims 12-19, 21-28, and 30-36; and amended claims 10-11 and claim 12 no longer recite that the GPP loads operands into the memory, none of the previously submitted claims provided a scope of coverage which is the same as, or comparable to, new reissue claims 12-19, 21-28, and 30-36.

In addition, new independent reissue claim 37 recites the invention as follows:

> 37. A data processing system comprising:
>
> a digital signal processor (DSP) that processes digital data by executing an algorithm that includes a specific sequence of DSP operations;
>
> a general purpose processor (GPP) that selects the sequence of DSP operations for execution by the DSP from a basic set of DSP operations, and that performs general purpose tasks utilizing selected instructions and data;
>
> a bus to which both the DSP and the GPP are connected;
>
> a memory connected to the bus such that the memory is accessible by the DSP for retrieving operands utilized by the DSP in executing the selected sequence of DSP operations and by the GPP for loading operands required for execution of the selected DSP algorithm and/or instructions and data for use by the GPP for controlling the DSP; and
>
> a control register of the DSP characterized in that said GPP invokes a first DSP operation in the selected sequence by issuing a corresponding command directly to said control register of the DSP.

Support for new reissue claim 37 may be found in FIG. 3, and column 6, lines 37-67 of the '153 patent specification.

As with new reissue claims 11, 20, and 29, new reissue claim 37 recites that the GPP loads operands into the memory, and that the DSP has a register, but does not recite either a bus interface unit or an external memory. As a result, none of the existing claims, and none of the previously submitted claims, provide a scope of coverage which is the same as, or comparable to, the scope of coverage provide by new reissue claim 37.

New dependent reissue claims 38-39 further recite the invention as follows:

> 38. The system of claim 37 wherein the DSP, in response to receiving a first DSP operation, places the GPP in a continuous wait state while the DSP performs the first DSP operation utilizing operands retrieved from the memory.
>
> 39. The system of claim 37 wherein, upon completion of execution of the selected sequence of the DSP operations, the GPP downloads contents of the memory and retrieves a new set of operands, instructions, and data for a new sequence of DSP operations.

Support for claims 38-39 may be found in column 8, lines 37-67 of the '153 patent specification.

Since existing claims 4-6 fail to recite that the GPP loads operands into the memory, none of the existing claims provide a scope of coverage which is the same as, or comparable to, the scope of coverage now provided by new reissue claims 38-39.

In addition, since originally-filed claims 10-14 recited elements which are not recited in new reissue claims 38-39, and amended claims 10-11 and claim 12 no longer recite that the GPP loads operands into the memory, none of the previously submitted claims

provided a scope of coverage which is the same as, or comparable to, new reissue claims 38-39.

Further, new independent reissue claim 40 recites the invention as follows:

> 40. A data processing system comprising:
> a first data bus;
> a second data bus;
> a memory connected to the first data bus and the second data bus;
> a general purpose processor (GPP) connected to the first data bus, the GPP loading operands into the memory via the first data bus; and
> a digital signal processor (DSP) connected to the first data bus and the second data bus, the DSP executing an instruction identified by the GPP, and retrieving operands from the memory via the second data bus.

Support for new claim 40 may be found in FIG. 3, and in column 6, lines 37-67 of the '153 patent specification.

None of the existing claims provide a scope of coverage which is the same as, or comparable to, the scope of coverage now provided by new reissue claim 40 as none of the existing and previously submitted claims recite a first memory and a DSP that are connected to both a first data bus and a second data bus.

New dependent reissue claims 41-44 further recite the invention as follows:

> 41. The data processing system of claim 40 wherein the operands held in the memory are randomly accessible.
>
> 42. The data processing system of claim 40 wherein the DSP places the GPP in a continuous wait state while the DSP executes the instruction.
>
> 43. The data processing system of claim 40 wherein the GPP reads a value that results from

executing the instruction after the DSP completes execution of the instruction.

44. The data processing system of claim 40 and further comprising:
a bus interface unit connected to the first data bus; and
a third data bus connected to the bus interface unit.

Support for new reissue claims 41-44 may be found in FIG. 3 and column 6, lines 37-67 of the '153 patent specification.

Since none of the existing claims, and none of the previously presented claims, recite a first memory and a DSP that are connected to both a first data bus and a second data bus, none of the existing claims, and none of the previously presented claims provide the scope of coverage provided by new reissue claims 41-44.

9. All errors being corrected in this reissue application up to the time of filing this declaration arose without any deceptive intention on my part.

10. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code and that such

willful false statements may jeopardize the validity of the application or any patent issued thereon.

Dated: July 12, 1998 By: [signature]
Moshe Doron